In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 7, 8, 16, 17, 19, 20, 27 and 28 without prejudice.

1. (Currently Amended) A computer system comprising:

a bus; and

a chipset, coupled to the bus, having:

an input/output (I/O) buffer, coupled to the bus, to transmit an output signal from the chipset via the bus;

a slew rate detection mechanism, coupled to the bus, to receive the output signal transmitted from the I/O buffer, to detect a slew rate of the output signal and to generate a signal indicating a status of the slew rate, including:

a reference current generator to generate a reference current;

a comparator to compare the received signal current to the reference current

a first converter to convert the signal current to a signal voltage; and

a second converter, coupled to the reference current generator and the comparator to convert the reference to a reference voltage; and

control logic, coupled to the slew rate detection mechanism, to receive the signal and to adjust the slew rate based upon the state of the signal.

2. (Cancelled)

3. (Cancelled)

4. (Previously Presented) The computer system of claim 1 wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast.

5. (Previously Presented) The computer system of claim 1 wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow.

6. (Previously Presented) The computer system of claim 1 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current.

7. (Cancelled)

8. (Cancelled)

9. (Original) The computer system of claim 6 wherein the comparator is an operational amplifier.

10. (Original) The computer system of claim 1 wherein the bus is a high-speed bus.

11. (Currently Amended) A computer system comprising:

a main memory device;

a memory bus coupled to the main memory device; and

a memory controller, coupled to the bus, having:

an input/output (I/O) buffer, coupled to the bus, to transmit an output signal from the memory controller via the bus;

a slew rate detection mechanism, coupled to the bus, to receive the output signal transmitted from the I/O buffer, to detect a slew rate of the output signal and to generate a signal indicating a status of the slew rate, including:

a reference current generator to generate a reference current;

a comparator to compare the received signal current to the reference current;

a first converter to convert the signal current to a signal voltage; and

a second converter to convert the reference to a reference voltage; and

control logic, coupled to the slew rate detection mechanism, to receive the signal and to adjust the slew rate based upon the state of the signal.

12. (Cancelled)

13. (Previously Presented) The computer system of claim 11 wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast.

14. (Previously Presented) The computer system of claim 11 wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow.

15. (Previously Presented) The computer system of claim 11 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current.

16. (Cancelled)

17. (Cancelled)

18. (Currently Amended) A method comprising:

transmitting a signal from an input/output (I/O) buffer within a chipset over a bus;

receiving the signal at a slew rate detection mechanism within the chipset via the bus;

generating a signal indicating the status of the slew rate

generating a reference current at the chipset;

converting the signal current to a signal voltage;

converting the reference current to a reference voltage; and

comparing the reference voltage to the signal voltage; and

adjusting the slew rate at control logic within the chipset based upon the signal.

19. (Original) The method of claim 18 further comprising.

20. (Original) The method of claim 19 further comprising:

21. (Original) The method of claim 18 wherein adjusting the slew rate comprises modifying the amplification of a second signal at the I/O buffer.

22. (Currently Amended) An apparatus comprising:

an input/output (I/O) buffer to transmit an output signal; and

a slew rate detection mechanism coupled to receive the output signal from the I/O buffer via a bus, to detect the slew rate of the output signal transmitted from the I/O buffer over a bus and to generate a signal to indicate the status of the slew rate, including:

a reference current generator to generate a reference current;

a comparator to compare the received signal current to the reference current;

a first converter to convert the signal current to a signal voltage; and

a second converter to convert the reference to a reference voltage.

23. (Cancelled)

24. (Currently Amended) The ~~computer system~~ apparatus of claim 22 further comprising control logic, coupled to the I/O buffer and the slew rate detection mechanism, to receive the signal and modify the slew rate based upon the signal.

25. (Cancelled)

26. (Original) The apparatus of claim 22 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current.

27. (Cancelled)

28. (Cancelled)